REMARKS

Claims 1, 2, and 4-35 are all the claims pending in the application. Claim 3 is canceled and claims 24-35 are added, above, to further define the invention. Claims 1, 2, and 4-23 stand rejected upon informalities and prior art grounds. In addition, the drawings are objected to. Applicants respectfully traverse these objections/rejections based on the following discussion.

I. Objections to the Drawings

The Office Action rejects Figs. 6A-6B, on the basis that the reference signs ATC, ATg, Slew_c and Slew_g are not described in the specification, and also, that all the labels in Fig. 11 are not described in the specification.

In response, Applicants direct the reader to paragraphs 0008-0009 of the specification which explains the reference to the arrival time (AT) and slew of the clock and gate using the following descriptions: AT_{clock} (ATc in the drawings), AT_{gate} (ATg in the drawings), $Slew_{clock}$ (Slew_c in the drawings), and $Slew_{gate}$ (Slew_g in the drawings). Applicants submit that one ordinarily skilled in the art would understand that the shorthand references in the drawings refer to the various clock or gate signal arrival times and slew periods. Therefore, Applicants respectfully submit that the specification as originally written provides support and sufficient description for the shorthand references used in Figures 6A-6B. Notwithstanding the foregoing, in order to speed prosecution and dispose of any ambiguities, paragraph 0008 has been amended to provide the forgoing description. This amendment to the specification does not add new matter because it merely describes what was previously shown in the drawings and specification.

Further, with respect to Figure 11, Applicants note that paragraph 0051 explains that Figure 11 is a graph showing the benefits produced by the invention. More specifically, the last sentence of paragraph 0051 explains that the histogram shown in Figure 11 demonstrates that the projected set up time minus the measured setup time provides a tighter distribution than the original propagated time for 2 input NAND clock gating. Paragraph 0051 describes that the data

shown in Figure 11 is computed over a very wide said of transistor widths, output capacitance loadings, and input slew. Therefore, Applicants submit that it would be clear to one of ordinary skill in the art that the number of occurrences shown in Figure 11 refers to the number of samples out of this very wide set. Further, the specification has been amended to clarify any ambiguity with respect to this issue. Once again, this amendment to the specification does not add new matter because it merely describes items previously illustrated and previously discussed in the specification. Further, Figure 11 merely demonstrates benefits of the invention (as opposed to claimed elements of the invention). Thus, Applicants respectfully submit that the benefits of the invention demonstrated by Figure 11 are explained in detail in the specification.

In addition, an inconsistency was noted in the specification and corrected with respect to Figure 11. More specifically, Figure 11 states that the measured set up time is subtracted from the projected setup time, while the specification incorrectly stated the inverse. Applicants submit that one ordinarily skilled in the art would have understood that the measured setup time would be subtracted from the projected setup time. Therefore, forgoing amendment to the specification does not add new matter.

II. The 35 U.S.C. 112, First Paragraph, Rejection

The Office Action rejects claims 1-23 under 35 U.S.C. 112, first paragraph, as not being described in the specification. In response, with respect to the issues discussed above for Figures 6A-6B and 11 (item 3a in the Office Action), Applicants make reference to the previous description. With respect to the waveforms shown in Figures 2-3 (item 3b in the Office Action), paragraphs 0005 and 0006 describe the operation of the clock gate and the manner in which it controls the output signal. Paragraphs 0005 and 0006 specifically describe the circumstances under which the output signal would be one or zero, and under which a clock pulse or portion of a clock pulse would be propagated to the gate input.

With respect to item 3c in the Office Action, Applicants submit that setup tests, hold tests, and clock gating tests are very well-known to those ordinarily skilled in the art. In addition,

paragraphs 0006 and 0007 explain these activities in sufficient detail to allow one ordinarily skilled in the art to make and use invention. With respect to item 3d in the Office Action, the terms ATc, ATg, Slew_c, and Slew_g are depicted in Figures 6A and 6B, and would easily be understood to be shorthand terms for AT_{clock}, AT_{gate}, $Slew_{clock}$, and $Slew_{gate}$ used in the computations referred to. Thus, for example, $Slew_{gate}/2$ would be understood by one ordinarily skilled in the art to mean that the $Slew_{gate}$ is divided by 2. Similarly, Figures 4 and 5 depict terms δ_g and δ_c, which are easily understood by one ordinarily skilled in the art to be shorthand for terms $delay_{gate}$ and $delay_{clock}$ in the various computations referred to in the Office Action, especially since δ is a commonly used shorthand symbol for delay. Further, the term K is described in detail in paragraph 0048 of the specification. With respect to item 3e in the Office Action, the specific identity of the signal attached to the lower input of the AND gate in Figure 8 was not described in the specification because it was not needed for illustrative purposes of the figure, which is to demonstrate that larger capacitive loading of a gate output increases delay when a transition on the output occurs due to an input transition, but does not increase the time required for input transitioning to the controlling state for a gate (e.g., zero for an AND gate) so as to prevent a transition on the output due to a subsequent transition on another input. In the context of the specification, which refers to clock gating, Applicants submit that it would be clear to one ordinary skill in the art that the upper input and the AND gate in Figure 8 is a clock input and that the lower input is a gating input.

In addition to forgoing descriptions and explanations, Applicants note that the Office Action does not relate the foregoing rejection to the claim language. Indeed, the terms which are questioned in section 3 of the Office Action do not appear in the claims. Therefore, it is unclear how the claims stand rejected as not being supported by the specification, when the rejection does not refer to the claim language. Applicants submit that the specification fully supports and describes the features defined by the claims. Therefore, Applicants respectfully submit that the claims are valid under 35 U.S.C. 112, first paragraph, and request that this rejection be withdrawn.

III. The 35 U.S.C. 112, Second Paragraph, Rejection

The Office Action rejects claims 1-3, 5, 11-13, and 17-19 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which Applicants regard as the invention.

With respect to the rejection of independent claims 1, 11, and 17, the Office Action indicates that dependent claim 3 is inconsistent with dependent claim 2 and that this causes confusion with respect to the first-type of signal and the second-type of signal. While Applicants respectfully disagree, dependent claim 3 has been cancelled without prejudice or disclaimer in order to eliminate any potential confusion in claims. In addition, modifications to Figures 2, 3, 5, 6A, and 6B are submitted herewith as proposed drawing corrections. These drawing corrections more clearly illustrate the first-type signal that enables output and the second-type signal that inhibits output. These proposed drawing corrections do not add new matter because paragraph 0005 explains that the high gate signal enables output and the low gate signal inhibits output (see the bottom of page 3 and top of page 4 of the specification). Applicants respectfully submit that with these corrections, the reader can clearly see that the invention does not alter the sensing of the output inhibiting signal (second-type of signal) but instead only changes the sensing of the output enabling signal (first-type of signal) as shown in Figure 6B. Therefore, once again, Applicants submit that the independent claims are clear and fully supported by the specification.

With respect to claims 5 and 6, Applicants again refer to paragraph 0005 which explains that one way to determine the correct setup or hold test between a pair of input signals to a gate is to simulate transitions on the input signals with a variety of different spacings (differences in arrival times), and find the minimum spacing which causes the gate to have the required output. Therefore, again, Applicants submit that the claims are supported by the specification.

Therefore, Applicants respectfully submit that the claims are valid under 35 U.S.C. 112, second paragraph, and request that this rejection be withdrawn.

IV. The Prior Art Rejection

Claims 1-23 stand rejected under 35 U.S.C. 102(a) as being anticipated by Wu (U.S. Patent No. 6,167,001). Applicants respectfully traverse these rejections because Wu is really directed to a process of successively changing the separation between signals until an error is detected in order to test the outer operating parameters of a given device. To the contrary, the claimed invention relates to sensing the enabling gating signal at an earlier point in time in order to reduce pessimism and permit more aggressive designs to test successfully.

More specifically, the abstract of Wu explains that the processing in Wu involves testing devices by repeatedly applying different pulses at progressive intervals until an error is detected. This finds, for example, the minimum signal delay under which the device being tested can properly operate. Wu is silent regarding reducing the slew calculation in order to sense enabling gating signal an earlier point in time, as the claimed invention does. To the contrary, Wu does not alter the way in which signals are sensed, but instead merely alters the timing between different signals.

Therefore, Wu does not teach or suggest the invention defined by independent claims 1, 11, and 17. More specifically, these claims define that the "first-type" signal enables the gating device to output a certain signal (e.g., a clock signal) and that the "second-type" signal inhibits the gating device from outputting such a signal. Then, in the last two lines of independent claims 1, 11, and 17, the invention provides a process of "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed." As explained in paragraph 0045 of the application, this feature of the invention reduces pessimism by reducing the delay calculation within a circuit.

More specifically, the delay savings can be seen when comparing Figures 6A and 6B. Figure 6A shows a fairly pessimistic situation wherein the midpoint 601 in the slew of the gate signal 110 must occur substantially before the midpoint 600 in the slew of the clock signal 100. The difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 is shown as time period 605. To the contrary, as shown in Figure 6B, by utilizing a

sensing point that is well in front of the midpoint 600, 601 (utilizing factor K, assuming no load, etc.), the invention is able to reduce the difference between the leading edge of the gate signal 110 and the leading edge of the clock signal 100 to a much smaller time 606. In other words, the invention is much less pessimistic and utilizes factor K to observe when the gate signal just begins its transition. Then, the invention is able to allow this sense point to occur just before when the clock signal begins its transition, as shown in Figure 6B. In doing so, the invention reduces timing delay requirements dramatically.

Wu does not and cannot teach these features because Wu does not alter when the rising clock signal is sensed. Instead, Wu progressively alters the delay between two separate signals in order to test the operational parameters of various devices. Therefore, Applicants respectfully submit that Wu does not teach or suggest "modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed" as defined by independent claims 1, 11, and 17. Thus, independent claims 1, 11, and 17 are not anticipated by Wu. Further, dependent claims 2, 4-10, 12-16, and 18-23 are similarly not anticipated by Wu, not only because they depend from a non-anticipated claimed, but also because of the additional features of the invention they define. In view the forgoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

V. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1, 2, and 4-35, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: _____

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